LAP TSL-A34

TWO-CHANNEL JFET LIMITER / COMPRESSOR · v0.3.2

LAP TSL-A34 is a two-channel JFET compressor / limiter built as a component-level circuit model. The plugin does not run a "compressor algorithm": the whole audio board (input followers, gain stage, the JFET-controlled stage, the precision rectifier, the attack / release network, the RATIO divider and the balanced output driver) is solved as a circuit in real time, component by component — including the operational amplifiers with their finite bandwidth, slew rate and input offsets, and the tolerances of the diodes and the FET, which make the two channels slightly different from each other, as two real boards are.

The two channels are two independent boards. **LINK** (the ON / OFF switch in the middle of the panel) makes channel 2 follow channel 1 for stereo work.

1 · Working the panel

Action	Result
drag a knob	vertical drag changes the value; hold `Shift` for fine control (1/10 speed)
hover a knob	the exact value is printed below the knob scale while the pointer is over the knob
double-click a knob	resets to default
click BYPASS	toggles the channel bypass; a lit (orange) button is bypassed. The switch cross-fades over 5 ms and the dry path is delay-matched, so it is click-free a
click ON / OFF	LINK — see §5
click the LAP logo	opens a small About window with the plugin version, formats and links; hovering the logo shows the version
right-click the panel	menu: Window (default 1189 × 162, 0.77× … 2×), Oversampling (1× / 2× / 4×), Character (Noise, Output transformer), Detector (Internal / External sidech

The panel follows the layout of a classic two-channel rack limiter: the two indicator LEDs sit in the top row, the control names are printed above the knobs, the range of each knob at the ends of its scale below it, and BYPASS sits to the left of the knob row at knob height. The knobs are the panel drawing with a rotating pointer (124 frames, 270° travel); the LINK slider, the BYPASS backlight and the light of the two LEDs are the only things drawn by code — the rest of the panel is the silkscreen.

2 · Controls (per channel)

Control	Range	Notes
GAIN	0 … +21.8 dB	gain of the input amplifier, *before* the controlled stage — it drives the signal into the threshold. 0 dB fully left; scale printed 0 … +22 dB.
ATTACK	0 … 100 %	position of the ATTACK pot (series resistor + pot into the envelope capacitors). Shortest fully left; scale printed 0.3 … 30 ms.
RELEASE	0 … 100 %	position of the 5 MΩ RELEASE pot (56 kΩ + 0…5 MΩ from the envelope capacitors). Shortest fully left; scale printed 0.2 … 2.5 s.
RATIO	3:1 … 10:1	the RATIO divider sets the DC offset of the control voltage — on this circuit it moves the **threshold** as much as the slope, see §3
OUTPUT	−8.4 … 0 dB	output level pot loaded by the balanced driver; 0 dB fully right (default), scale printed −8 … 0 dB
BYPASS	ON / OFF	the board's own bypass: the clean signal from the input differential amplifier goes straight to the output driver, delay-compensated

> **ATTACK and RELEASE are pot positions, not milliseconds.** Measured on the gain reduction with a 20 dB step at 4:1, the network gives attack ≈ 0.3 ms (min) … 30 ms (max) to 90 % and release ≈ 0.2 s (min) … 2.5 s (max) to within 1 dB — these are the figures printed at the ends of the knob scales. Short settings are fast enough for limiting, long ones are programme-friendly; the hover read-out stays in percent of travel.

3 · Levels, threshold and ratio

The plugin is calibrated so that **0 dBFS = 4.4 V peak** on the balanced input. The circuit's threshold (1.1 V rms, set by the internal trimmer) therefore sits at **−9 dBFS with RATIO at 10:1** and moves down to about −15 dBFS at 3:1. Below threshold the board passes the signal at unity (the 20 Hz – 20 kHz response of the coupling network is within ±1 dB).

input dBFS	3:1	4:1	6:1	10:1
−24	−24.6	−24.6	−24.6	−24.6
−15	−16.8	−15.6	−15.6	−15.6
−12	−16.4	−14.8	−12.6	−12.6
−9	−15.8	−14.4	−12.1	−9.6
−6	−15.2	−14.0	−11.9	−8.4
0	−13.7	−12.8	−11.1	−8.1

Output level [dBFS] for a 1 kHz sine, GAIN 0 dB, OUTPUT 0 dB, steady state.

The knee is hard and the slope above the threshold is steep (about 5–6:1 at every RATIO setting; the printed 3:1 … 10:1 describes the whole curve from 0 to +15 dB over the threshold). Turning RATIO towards 3:1 is the way to get *earlier, gentler* action: the threshold drops and the first decibels are

compressed softly. GAIN is the drive control: with the threshold fixed, GAIN decides how far into the limiter the programme goes; use OUTPUT to bring the level back.

Above the threshold the JFET adds a little harmonic distortion (about 0.8 % at 4 dB over, mostly second harmonic) — that is the sound of the circuit, not an added effect.

4 · Sound and character

Below the threshold the board passes the signal at unity and is very clean: the harmonic distortion is that of the amplifier chain — in the order of 0.001 % at 1 kHz, rising towards 0.02 % at 8 kHz as the loop gain of the amplifiers falls. Above the threshold the JFET takes over: about 1 % second harmonic at 1 kHz a few dB into limiting, and at low frequencies the ripple of the envelope modulates the gain within the cycle (several percent at 63 Hz when driven hard) — the classic sound of a fast feedback limiter.

Option (right-click)	Default	What it does
Noise	on	the noise of the input stage and the amplifiers, about −104 dBFS at GAIN 0 dB and rising with GAIN, white. Part of the model; switch it off for silent stems.
Output transformer	on	a LAP addition: a saturating line transformer stage after the output driver (core hysteresis solved sample by sample, 4× oversampled). Adds low-frequency weight and second/third harmonic that grows as the level and the bass content rise. On by default; switch it off for a clean line output. Adds 36 samples of latency.

First hit after a pause. This is a feedback limiter: with no signal the control voltage sits well below the JFET pinch-off, so after a few seconds of silence the gain element is fully open and the first transient passes at full GAIN until the detector has charged the envelope past the threshold — a millisecond or so at ATTACK minimum, a few tens of milliseconds at ATTACK maximum, and longer towards 3:1 where the idle control voltage sits deepest. After that the loop settles and later hits are caught normally. It is part of the character of a feedback limiter, not a fault; if you need every first hit caught, keep some signal running into the unit, or use a look-ahead limiter after it.

The two channels use two sets of component tolerances (diode currents, FET pinch-off, amplifier offsets), so with LINK on the panel edits both, but they are not bit-identical — as two channels of one unit never are.

5 · LINK and the two channels

The **ON / OFF** slider in the middle of the panel is LINK (default ON). With LINK on, every knob and BYPASS of channel 1 is mirrored to channel 2 and the panel edits both at once; channel 2's own settings are copied from channel 1 the moment you switch LINK on, so nothing jumps when you switch it off again.

With LINK off the unit is dual mono: two boards, two sets of controls, no interaction between the channels.

6 · LIMIT and GAIN indicators

Each channel has two LEDs in the top row of the panel, above the LIMIT and GAIN captions. The red **LIMIT** LED lights while the channel is reducing gain by 0.5 dB or more (with a short hold so brief peaks are visible). The green **GAIN** LED is the overload indicator of the input amplifier: it lights when the GAIN stage is driven to its negative rail (about −11 V). When it flickers on programme, turn GAIN down — the stage is clipping before the compressor.

7 · Sidechain

The plugin has an auxiliary input named **Sidechain** (stereo, or mono in the mono layout). Right-click the panel and choose **Detector → External sidechain**, or use the host parameter **Ext Sidechain**. The rectifier of the control path (VD11 / VD12) is then disconnected from the board's own output and fed from the aux input at the same calibration (0 dBFS = 4.4 V).

> **This is a feedback compressor.** Its detector listens to the already-compressed output, which is what limits the slope. With an external key the loop becomes feed-forward from that key: for the same level over the threshold the gain reduction is deeper (about 16 dB instead of 10 dB at +12 dB over), and with nothing connected to the aux input the channel simply does not compress. There is no automatic fallback — switch the detector back to *Interna/* when the key is gone. In the DAW the key must actually be routed to the plugin's Sidechain input (VST3: the second input bus; CLAP: the aux port) — a track that only plays next to it is not a key.

8 · Oversampling and CPU

The default is **1×**: the circuit is integrated with the trapezoidal rule at the host rate. The poles of the board that lie above half the sample rate would be warped by that integration into a roll-off near 20 kHz, so at 1× the plugin compensates for it with a small fixed equaliser — the response then follows the circuit to within 0.1 dB up to 0.375 × the sample rate (18 kHz at 48 kHz) and rolls off gently above (−0.8 dB at 19 kHz, −3 dB at 20 kHz at 48 kHz), which also keeps aliasing products near the Nyquist frequency from being lifted. **2×** needs no compensation and pushes the aliasing products of hard limiting further out, at twice the cost; **4×** is for 44.1 kHz sessions with very bright material. The choice is saved with the session.

The board is solved as seven small circuit stages in signal order (input stage, GAIN amplifier, controlled stage with the JFET, output driver, rectifier, envelope, RATIO / control voltage), each its own nodal system — the same physics as one big matrix, at a fraction of the cost.

Stereo, 48 kHz	1×	2×	4×
share of one core, 1 kHz tone	≈ 25 %	≈ 38 %	≈ 59 %
drums, GAIN +20 dB	≈ 40 %	≈ 56 %	≈ 79 %
latency (samples)	0	30	36

Measured on the development machine, one core; the output transformer adds 36 samples of latency and a few percent. Oversampling multiplies only the audio stages (input, GAIN, JFET stage, output driver); the detector — rectifier, envelope and control voltage — always runs at the host rate, so 4× costs about 2.5× rather than 4×. The two channels are two independent models and are computed on two threads, so the figures above are the total — per core it is about half, and a mono instance computes one channel only. 4× is still the heaviest setting — use it for bounces or a single bus, not on every track. The gain reduction, threshold and ratio are identical at 1×, 2× and 4×; only the top-octave response and aliasing differ.

9 · Signal flow

Stage	What happens
input	balanced input, RF filter, PNP emitter followers, differential input amplifier (unity)
GAIN	inverting gain stage, 22 kΩ + 250 kΩ pot → 0 … +21.8 dB (its output drives the GAIN LED)
controlled stage	summing amplifier with a non-inverting helper stage; the JFET shunts the ground leg of the helper and takes up to ~17 dB out of the loop
OUTPUT · BYPASS	10 kΩ output pot → BYPASS switch → balanced output driver
detector	from the output node (or the Sidechain input): precision full-wave rectifier → diode + ATTACK pot charge / diode + RELEASE pot discharge of 2 × 1 µF → bu
RATIO / CV	the control amplifier sums the envelope with the RATIO divider offset (−3.4 … −8.4 V) → diode → JFET gate
after the board	1×: integration-warping compensation · optional output transformer (4× oversampled)